

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Patent Application of:	)	Confirmation No.: 9417
Shunpei YAMAZAKI et al.	)	Group Art Unit: 2894
Application No.: 10/576,420	)	Examiner: Tony Tran
Filed: April 19, 2006	)	
For: LIQUID CRYSTAL DISPLAY DEVICE AND	)	Date: <u>March 1, 2010</u>
METHOD FOR MANUFACTURING THE SAME	)	

**PRE-APPEAL BRIEF REQUEST FOR REVIEW**

**Mail Stop: AFTER FINAL**  
Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450

Sir:

Pursuant to the Pre-Appeal Conference Pilot Program, and further to the Examiner's Final Office Action dated December 1, 2009, Applicants hereby file this Pre-Appeal Brief Request for Review. This Request is accompanied by the concurrent filing of a Notice of Appeal.

Applicants hereby request formal review of the Final Office Action mailed December 1, 2009. In particular, the Examiner has maintained an improper rejection of claims 1, 19-24, 26-34, 36, and 37 under 35 U.S.C. § 103(a) as allegedly being unpatentable over Arao et al. (U.S. Patent No.: 6,639,265 B2) (*Arao*, hereinafter) in view of Japanese patent document 2003-318133 (*JP '133*, hereinafter), and in further view of Kobayashi et al. (U.S. Pub. No.: 2002/0006558 A1) (*Kobayashi*, hereinafter).

In an effort to overcome the above rejections, Applicants have amended the claims to include specific, tangible characteristics of the claimed invention. Each of the claims recite a specific combination of features that distinguishes the invention from the prior art in different ways. Specifically, independent claim 1 is directed to a liquid crystal display device including, *inter alia*, the features of:

“...a projection comprising a conductive material formed over at least one of a drain electrode and a source electrode of the thin film transistor;  
an interlayer insulating film formed over the thin film transistor; and  
a pixel electrode connected to the projection,  
wherein the interlayer insulating film is interposed between the base film and the pixel electrode,  
wherein the projection has a stacked structure including a plurality of conductors and  
**wherein each of the plurality of conductors is in direct contact with the interlayer insulating film.”** (Emphasis added)

Independent claim 26 is directed to a liquid crystal display device including, *inter alia*, the features of:

“...a first projection comprising a conductive material formed over at least one of a drain electrode and a source electrode of the thin film transistor;  
an interlayer insulating film formed over the thin film transistor; and  
a pixel electrode connected to the first projection;  
a terminal portion comprising...  
a second projection comprising a conductive material formed over the second wiring;  
a second insulating film formed over the second wiring; and  
a terminal electrode connected to the second projection,  
wherein the interlayer insulating film is interposed between the base film and the pixel electrode,  
wherein each of the first projection and the second projection has a stacked structure, said first projection including a plurality of first conductors and said second projection including a plurality of second conductors; and  
**wherein each of the plurality of first conductors is in direct contact with the interlayer insulating film and each of the plurality of second conductors is in direct contact with the second insulating film.”**

At the very least, the applied *Arao*, *JP '133*, and *Kobayashi* references, taken either alone or in combination, fail to disclose, teach, or suggest the above-identified features recited, e.g., in independent claims 1 and 26. Applicants have further included explanations of the distinctions between the present invention and that of the Examiner's purported prior art combination. However, despite Applicants' attempts to overcome these rejections, the Examiner continues to

maintain that although *Arao* “does not disclose wherein each of the plurality of conductors is in direct contact with the interlayer insulating film, “[n]evertheless, ‘133 does teach a light emitting element part (140a, [Drawing 23], page 34 of 47) wherein each of the plurality of conductors (142, 144, [0156]) is in direct contact with the interlayer insulating film (148, [0155]).”<sup>1</sup>

However, this rejection is erroneously applied under 35 U.S.C. § 103(a), because the structures of *Arao*, *JP ‘133*, and *Kobayashi*, taken either alone or in combination, fail to disclose, teach, or suggest each and every feature recited in the pending claims in accordance with M.P.E.P. § 2143.03, to thereby establish a *prima facie* case of obviousness with respect to the invention as claimed.

Applicants had previously directed the Examiner to paragraph [0156] of the machine translation of *JP ‘133*, which shows that item 142 is an electron hole transportation/pouring layer and item 144 is a luminous layer.<sup>2</sup> Consequently, the combination of *Arao* and *JP ‘133* would appear to yield a light emitting element rather than a source or drain wiring formed between the thin film transistor 204 and the pixel electrode 156 in *Arao*.<sup>3</sup>

Moreover, as seen in Drawings 20C-D of *JP ‘133*, e.g., an electric conduction film 112 is interposed between insulating films 114, as delineated in the explanation of letters or numbers section of the machine translation. Consequently, even if it were proper to combine *Arao* and *JP ‘133*, which Applicants assert that it is improper, it would appear that in *Arao* the thin film transistor 204 would not be electrically connected to the pixel electrode 156. Thus, in combining the device of *JP ‘133* with that of *Arao* would actually render *Arao*’s device unworkable.

The Examiner failed to provide a response to the arguments that have been reasserted above in the Office Action mailed December 1, 2009. Rather, the Examiner merely stated that “the main purpose of combining [*Arao*] with ‘133 is the projection [P] is formed by **DROPLET DISCHARGE METHOD** wherein when this method is used, it inherently teach

<sup>1</sup> See the Office Action, e.g., page 4.

<sup>2</sup> See *JP ‘133*, e.g., paragraph [0156] and FIG. 23.

<sup>3</sup> See *Arao*, e.g., FIG. 5A and col. 12, ll. 7-27.

wherein each of the plurality of layers (142, 144, [0156], note that this inherency characteristic are disclosed in Applicant' specification [the tapered shape which come from ONE conductive material 43 as shown in FIGS. 1C-1E]) is in direct contact with the interlayer insulating film (148, [0155]).”<sup>4</sup>

However, it appears that the Examiner has used impermissible hindsight in attempting to reconstruct the presently claimed invention based upon information that the Examiner has gleaned from Applicants' disclosure. Especially, since *Arao* does not teach or suggest a droplet discharge method, and the Examiner's combination of *Arao* with *JP '133* is deficient for at least the above-identified reasons. Furthermore, the disclosure of *Kobayashi* fails to remedy the above-identified deficiencies with respect to *Arao* and *JP '113*.

Accordingly, these deficiencies, of the cited prior art, are in clear contradiction of the M.P.E.P., which requires the Examiner to provide a showing of the existence of any reasonable probability of success in modifying *Arao*, the base reference, at least on teachings of *JP '133* and *Kobayashi* in order to establish a *prima facie* case of obviousness. In view thereof, it is clearly improper to maintain an obviousness rejection of the independent claims 1 and 26 under 35 U.S.C. § 103(a) in view of *Arao*, *JP '133*, and *Kobayashi*, taken either alone or in any proper combination. Therefore, Applicants respectfully submit that this rejection should be withdrawn.

The rejection of claims 19-24, 27-34, 36, and 37 should also be withdrawn due to the dependency of these claims, either directly or indirectly, from either independent claim 1 or 26, but also because claims 19-24, 27-34, 36, and 37 are distinguishable over the prior art.

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<sup>4</sup> See the Office Action, e.g., page 13.

In view of the foregoing remarks, it is respectfully submitted that the present application is in condition for allowance, and prompt notification of the same is earnestly sought.

Respectfully submitted,

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Date: March 1, 2010

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94306-2022